1. A circuit comprising:

a first edge-to-pulse converter having a first input to receive an initiating signal and a second input to receive a terminating signal, the first edge-to-pulse converter to provide an intermediate initiating signal at an output; and

a second edge-to-pulse converter having a first input to receive the intermediate initiating signal and a second input to receive the terminating signal, the second edge-to-pulse converter to provide a pulse having a width determined by a first edge of the intermediate initiating signal and a first edge of the terminating signal.

2. The circuit of claim 1, wherein each of the first and second converters performs an AND operation on the signals applied to its first and second inputs.

3. The circuit of claim 2, wherein the AND operation is performed by first and second transistors coupled in series and having a first conductivity type, the gates of the first and second transistors forming the first and second inputs of the converters.

4. The circuit of claim 3, wherein each of the first and second converters further includes a pre-charge transistor coupled in series with the first and second transistors, a gate of the pre-charge transistor being coupled to the second input of its respective converter.

5. The circuit of claim 4, wherein the initiating and terminating signals are start and stop pulses, respectively, and the width of the intermediate initiating signal is determined by edges of the start and stop pulses.

6. The circuit of claim 1, wherein a trailing edge of the intermediate initiating signal is determined by a leading edge of the stop pulse.

7. The circuit of claim 1, wherein the first converter includes first, second and third transistors coupled in series between first and second reference voltages and an inverter coupled to a drain of the first transistor and the converter output.

8. The circuit of claim 7, wherein the first input is coupled to a gate of the second transistor and the second input is coupled to gates of the first and third transistors.

9. A method comprising:

initiating an intermediate signal responsive to detection of an initiating signal;

terminating the intermediate signal, responsive to detection of a terminating signal;

initiating an output signal, responsive to detection of the intermediate signal; and

terminating the output signal, responsive to detection of the terminating signal.

10. The method of claim 9, wherein initiating the intermediate signal comprises initiating the intermediate signal responsive to a leading edge of the initiating signal.

11. The method of claim 9, wherein terminating the intermediate signal comprises terminating the intermediate signal responsive to a leading edge of the terminating signal.

12. The method of claim 11, further comprising generating the terminating signal a selected interval following the initiating signal, the selected interval corresponding to a desired width of the output signal.

13. A circuit comprising:

a start pulse source to generate a start pulse having a width;

a stop pulse source to generate a stop pulse having a delay relative to the start pulse, determined by a bit;

a first edge-to-pulse converter to generate an intermediate pulse having a width determined by the start pulse and a first edge of the stop pulse; and

a second edge-to-pulse converter to generate a symbol having a width determined by a first edge of the intermediate pulse and the first edge of the stop pulse

14. The circuit of claim 13, wherein the first edge-to-pulse converter includes an AND gate that is driven by the start and stop pulses.

15. The circuit of claim 14, wherein the second edge-to-pulse converter includes an AND gate that is driven by the intermediate and stop pulses.

16. The circuit of claim 13, wherein the stop pulse source includes a sequence of delay modules that may be sampled at selected locations of the sequence to provide the selected delay.

17. A method comprising:

initiating an intermediate signal, responsive to a first programming signal;

initiating an output signal, responsive to the intermediate signal;

terminating the output signal, responsive to a second programming signal; and

terminating the intermediate signal, responsive to an event associated with the second programming signal.

18. The method of claim 17, wherein terminating the intermediate signal comprises:

detecting a leading edge of the second programming signal; and

terminating the intermediate signal responsive to detecting the leading edge of the second programming signal.

19. The method of claim 17, wherein terminating the intermediate signal comprises:

detecting a trailing edge of the output signal; and

terminating the intermediate signal responsive to detecting the trailing edge of the output signal.

20. The method of claim 17, wherein the event associated with the second programming signal is expiration of an interval that exceeds a delay between the first programming signal and a latest second programming signal, and terminating the intermediate signal comprises terminating the intermediate signal responsive to expiration of the interval.

21. The method of claim 17, wherein the event associated with the second programming signal is expiration of an interval that is less than a delay between the first programming signal and an earliest second programming signal, and terminating the intermediate signal comprises terminating the intermediate signal responsive to expiration of the interval.

22. A circuit comprising:

a first module having first input to receive a first programming signal, a second input to receive a terminate signal, the first module to initiate an intermediate signal responsive to the first programming signal and to terminate the intermediate signal responsive to the terminate signal; and

a second module having a first input to receive the intermediate signal and a second input to receive a second programming signal, the second module to initiate and terminate an output signal, responsive to the intermediate signal and the second programming signal, respectively, wherein the terminate signal for the first module is related to the second programming signal.

23. The circuit of claim 22, wherein the terminate signal for the first module is the second programming signal.

24. The circuit of claim 23, wherein the first module terminates the intermediate signal responsive to a leading edge of the second programming signal.

25. The circuit of claim 22, wherein the terminate signal for the first module is related to the output signal.

26. The circuit of claim 25, wherein the first module terminates the intermediate signal responsive to a trailing edge of the output signal.